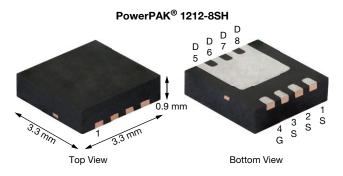
SiSH106DN

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Vishay Siliconix

N-Channel 20 V (D-S) Fast Switching MOSFET



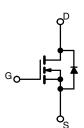
FEATURES

- TrenchFET[®] power MOSFET
- 2.5 V rated R_{DS(on)}
- PWM optimized
- 100 % R_a tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Synchronous rectification
- Load switch

PRODUCT SUMMARY						
V _{DS} (V)	20					
$R_{DS(on)}$ max. (Ω) at V_{GS} = 4.5 V	0.0062					
$R_{DS(on)}$ max. (Ω) at V_{GS} = 2.5 V	0.0098					
Q _g typ. (nC)	17.5					
I _D (A)	19.5					
Configuration	Single					



RoHS

COMPLIANT

HALOGEN

FREE

N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8
Lead (Pb)-free and halogen-free	SiSH106DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS	(T _A = 25 °C, unle	ss otherwise n	ioted)		
PARAMETER	SYMBOL	10 s	STEADY STATE	UNIT	
Drain-source voltage		V _{DS}	20	20	V
Gate-source voltage		V _{GS}	± 12 ± 12		V
Continuous drain current (T _J = 150 °C) ^a	T _A = 25 °C		19.5	12.5	
	T _A = 70 °C	I _D	15.6	10	
Pulsed drain current		I _{DM}	60	60	A
Continuous source current (diode conduction) ^a		I _S	3.2	1.3	
Single avalanche current		I _{AS}	30	30	
Single avalanche energy	L = 0.1 mH	E _{AS}	45	45	mJ
Maximum neuror dissinction a	T _A = 25 °C	PD	3.8	1.5	W
Maximum power dissipation ^a	T _A = 70 °C		2	0.8	VV
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) ^{b, c}			2	260	-0

THERMAL RESISTANCE RATINGS						
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction to ambient a	t ≤ 10 s	R _{thJA}	24	33	°C/W	
Maximum junction-to-ambient ^a	Steady state		65	81		
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.9	2.4		

Notes

a. Surface mounted on 1" x 1" FR4 board

See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK 1212-8SH is a leadless package within the PowerPAK 1212-8 package family. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at b. the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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SPECIFICATIONS ($T_J = 25$ °	C, unless otł	nerwise noted)				
PARAMETER	METER SYMBOL TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	0.6	-	1.5	V
Gate-body leakage	I _{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V	-	-	± 100	nA
Zoro gato voltago drain current	L	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	V _{GS} = 0 V 1		1	
Zero gate voltage drain current	IDSS	V_{DS} = 20 V, V_{GS} = 0 V, T_J = 55 °C	-	-	5	μA
On-state drain current ^a	I _{D(on)}	$V_{DS} \geq 5 \text{ V}, V_{GS} = 4.5 \text{ V}$	40	-	-	А
Drain-source on-state resistance ^a	В	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 19.5 \text{ A}$	-	0.0051	0.0062	Ω
	R _{DS(on)}	$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 15.5 \text{ A}$	-	0.0081	0.0098	52
Forward transconductance ^a	9 _{fs}	$V_{DS} = 15 \text{ V}, \text{ I}_{D} = 19.5 \text{ A}$	-	105	-	S
Diode forward voltage ^a	V _{SD}	$I_{\rm S} = 3.2$ A, $V_{\rm GS} = 0$ V	-	0.8	1.2	V
Dynamic ^b						
Total gate charge	Qg		-	17.5	27	
Gate-source charge	Q _{gs}	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 19.5 A	-	6.6	-	nC
Gate-drain charge	Q _{gd}		-	2.8	-	
Gate resistance	R _g	f = 1 MHz	0.7	1.4	2.1	Ω
Turn-on delay time	t _{d(on)}		-	25	40	
Rise time	t _r	V_{DD} = 10 V, R_{L} = 10 Ω	-	15	25	
Turn-off delay time	t _{d(off)}	$I_D \cong 1 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 6 \Omega$	-	50	75	ns
Fall time	t _f		-	12	20	
Source-drain reverse recovery time	t _{rr}	I _F = 3.2 A, di/dt = 100 A/μs	-	30	60	

Notes

a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

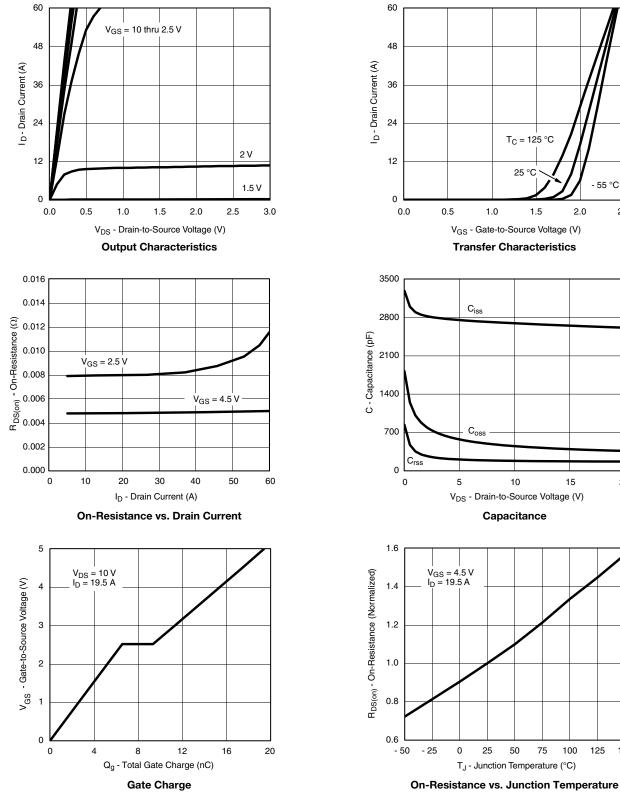
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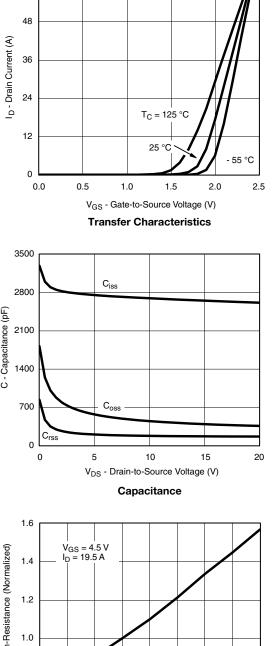


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





0

25

50

T_J - Junction Temperature (°C)

75

100

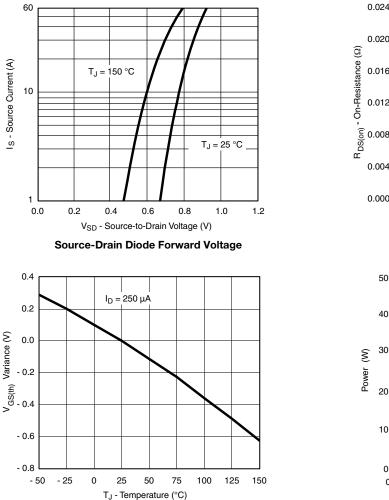
125 150



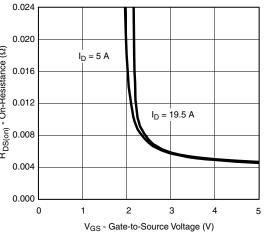
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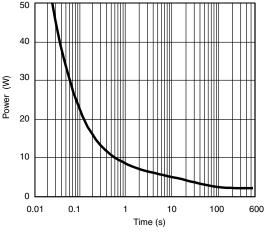
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



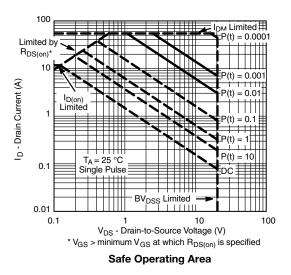
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



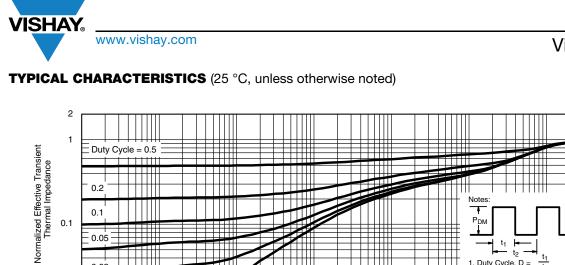




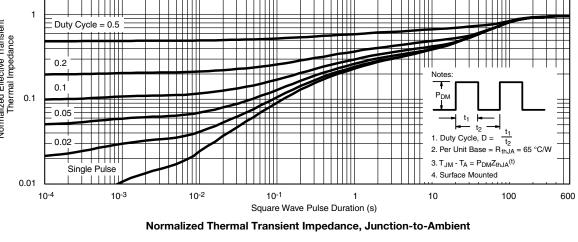
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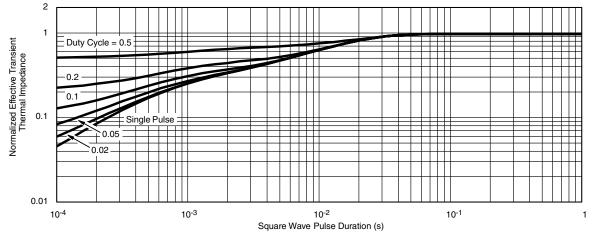
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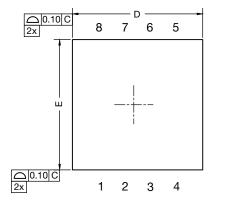
Normalized Thermal Transient Impedance, Junction-to-Case

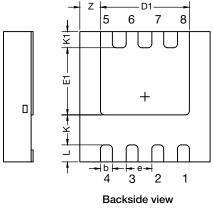
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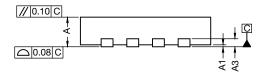


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PowerPAK[®] 1212-SWLH







DIM		MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN. NOM.	MAX.			
А	0.82	0.90	0.98	0.032	0.035	0.038		
A1	0	-	0.05	0	-	0.002		
A3		0.20 ref.			0.008 ref.			
b		0.30 BSC			0.012 BSC			
D	3.30 BSC			3.30 BSC 0.130 BSC				
D1	2.15	2.25	2.35	0.084	0.088	0.092		
E		3.30 BSC		0.130 BSC				
E1	1.60	1.70	1.80	0.063	0.067	0.071		
е		0.65 BSC			0.026 BSC			
к		0.76 typ.			0.030 typ.			
K1		0.41 typ.			0.41 typ. 0.016 typ.			
L		0.43 BSC			0.017 BSC			
Z		0.525 typ.			0.021 typ.			



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